Hierarchical design partitioning of digital systems for 3D system integration

Students: Electronics / Computer Engineers
Type: Experimental
Required skills: Various programming skills (OO, C/C++)

MOTIVATION

Current 3D integrated circuits can be implemented using traditional synthesis and place & route tools. However, the current Electronic Design Automation (EDA) tools do not support simultaneous design of multiple die databases in the same run (placement problem is always reduced to 2D).

To overcome this important limitation, current EDA solution consists in treating the system as two (or more) separate netlists, one per die in the system plus one top-level netlist that instantiates all the others. Each netlist is then implemented separately, as an independent design.

Generating such netlists before the logic synthesis could be very complex, since design hierarchy is already established and in most cases is very complex. Doing manual partitioning of the netlist after synthesis is not a workable solution either due to connectivity complexity and the number of instances in the system. Therefore, there is a need for automation of this task. Based on existing open-source parser for Verilog netlists, we have developed an initial version of such partitioning tool. However, the current implementation supports only flat netlist at its input. As of today, this can be seen as a limitation, since in certain cases design hierarchy should be preserved.

OBJECTIVES

- Based on existing Verilog parser add the capability of hierarchical netlist partitioning
- If the current parser shows limitations in terms of execution time, we could foresee a C/C++ implementation of a hierarchical Verilog parser
- Benchmarking and software optimization to handle large netlists in reasonable computational time

CONTACT

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Physical-layer security — IoT device authentication and ciphering using physical unclonable functions

Students: Electronics / Computer Engineers, Cybersecurity scientists
Type: Theoretical and/or experimental

MOTIVATION

There are approximately 7 billion of IoT devices in the world today and their number grows aggressively over the years. With their large level of deployment comes the need of protecting these devices from malicious since IoT (in)security is a major problem and a rising threat (see for instance the Mirai botnet attack). In practice, there is a strong need to implement lightweight authentication and ciphering of the communication beyond classical crypto protocols, such as Diffie-Hellman key exchange or TLS that are out of the reach of embedded electronics.

A physical unclonable function (PUF) is a device that exploits inherent randomness introduced during CMOS manufacturing to give a physical entity a unique fingerprint of the device (similar to human biometrics). PUFs are most often based on unique physical variations which occur naturally during semiconductor manufacturing but can also be embodied in side electronics designed for that purpose. Examples include clock drifts, SRAM memory states at power-up, logical gates response, etc.

From a security perspective, any challenge presented to a device will lead to a different response, based on the unique characteristics of the electronics (see fig. below) and can be exploited to perform identification, signing, and key derivation.

OBJECTIVES

- Understand the core concepts of physical unclonable function and its application in the context of Internet of Things.
- Demonstrate using a FPGA-based implementation and analyse its sensitivity to the environment (e.g. power-up cycles, temperature).
- Identify your device with its unique fingerprint and the corresponding fuzzer (a “correction” function to stabilize the input and output)

CONTACT

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Physical-layer security — Physical unclonable functions from and for commodity hardware

Students: Electronics / Computer Engineers, Cybersecurity scientists
Type: Theoretical and/or experimental

MOTIVATION

There are approximately 7 billion of IoT devices in the world today and their number grows aggressively over the years. With their large level of deployment comes the need of protecting these devices from malicious since IoT (in)security is a major problem and a rising threat (see for instance the Mirai botnet attack). In practice, there is a strong need to implement lightweight authentication and ciphering of the communication beyond classical crypto protocols, such as Diffie-Hellman key exchange or TLS that are out of the reach of embedded electronics.

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From a security perspective, any challenge presented to a device will lead to a different response, based on the unique characteristics of the electronics (see fig. below) and can be exploited to perform identification, signing, and key derivation.

OBJECTIVES

- Understand the core concepts of physical unclonable function and its application in the context of Internet of Things.
- Investigate how commodity hardware can be exploited / extended in order to embed PUF.
- Deliver an implementation on a RaspberryPi box.

CONTACT

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Indoor localization and navigation using ultra-wideband ranging

Motivation and context

Localization relies largely on GNSS technology, such as GPS, Galileo or Glonass. However, GNSS systems are unreliable in indoor environments, such as buildings, which is a real problem for indoor navigation systems. Ultra-wideband (UWB) is an emerging wireless technology that allows to estimate the distance between two UWB tags with centimeter-like accuracy. UWB has reached the level of maturity required to use it in many applications, including indoor navigation systems.

Figure: Localization setup using three anchors, and screenshot of the current Android app

Objective

The aim of this thesis is to continue the development of an indoor navigation system on a smartphone. The current version of the system is able to localize a tag in an indoor environment with an accuracy of ~50cm (see screenshot above), and to estimate the orientation of the smartphone using the smartphone inertial measurement unit. In order to make it into a full-fledged navigation system, a whole list of tasks needs to be performed:

- Outsourcing the low-level tasks (that are currently done in the Android OS) to an external microcontroller
- Designing and implementing a MAC protocol that will allow to use many tags simultaneously
- Designing and implementing Kalman filters to improve the tag’s localization and orientation
- Integrate open-source navigation SDKs to include the possibility of navigation into the app
- Design a PCB to integrate the microcontroller, UWB tag and associated electronics
- Using the wireless channel estimation to account for multipath to improve localization performance
- Implement the software for the anchors using a real-time OS (FreeRTOS) on ESP8266 modules
- ...

Most of the programming will be done in Java (Android's programming language) and in C for the microcontrollers.

Supervisor: Prof. François Quitin (ULB)

Information: François Quitin (fquitin@ulb.be) Tel: 02-650-2829, BEAMS Department

Students: ELEC, INFO, EM
Localization of RF transmitters using sensor fusion

Motivation
Localization of RF transmitters in wireless networks is a widely-investigated topic with countless applications for industry, security and advertisement purposes. The use of multiple-antenna arrays for direction-of-arrival (DoA) estimation of RF transmitters has been widely considered for localization. However, the high cost associated with the manufacturing of multi-antenna arrays and the form factor constraints of multi-antenna arrays prohibit their widespread use in portable consumer electronics.

In this project, we propose to use a mobile, single-antenna receiver to estimate the DoA of a RF transmitter (see my talk at FOSDEM 2017 for more information: http://mirrors.dotsrc.org/fosdem/2017/AW1.120/multiantenna.mp4)

Concept of virtual multi-antenna array for DoA estimation

Objectives
This project aims at prototyping the proposed method on an embedded software-defined radio testbed. We will use a USRP-E310, which contain a Xilinx 7 series FPGA and an integrated ARM A9 processor, as well as a 9-axis IMU. The FPGA can be programmed to track the phase of the received RF messages, whereas the embedded processor can be used to compute the IMU navigation solution and estimate the final DoA. A separate transmitter will be used as a transmitter, and the USRP-E310 will be used as receiver to estimate the transmitter DoA.

Previous work provided an off-line implementation, the objective of this thesis is to offer a real-time prototype, and perform an evaluation of the performance of virtual DoA estimation in different scenarios.

Supervisor: Prof. François Quitin

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Students: ELEC, INFO
Design of a 28 GHz transceiver chain for 5G systems

Motivation
5G networks will include a wide array of new technologies and concepts, including the use of new carrier frequencies. 28 GHz will be used for picocell communications, offering large bandwidths and large multi-antenna arrays.

![Example of a X-MWsystem fast-prototyping assembly](image)

Objective
This master thesis will have to design and test a 28 GHz transceiver system. The student will have to design, assemble and test the 28 GHz up- and down-converters. The student will then have to integrate two 4x4 28 GHz arrays and write the software to control these arrays. Finally, the student will have to use the setup to demonstrate the communication performances, but also the localization performances by using the beamforming capabilities of the phased arrays.

Supervisors: Prof. François Quitin, Prof. Philippe De Doncker

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Students: ELEC
Design of a RF user localization system for smart cities

Motivation
Smart cities entail the real-time monitoring of traffic in urban environments. A promising approach for estimating the positions and speeds of targets (pedestrians, bikes, and cars) is the combination of different technologies. One of such technology is based on passive WiFi systems that opportunistically acquire WiFi signals transmitted by smartphones and process them to estimate user positions and speeds. These WiFi systems rely on estimating the direction of the transmitter (using angel-of-arrival estimation), or by estimating the distance of the transmitter (using time-difference-of-arrival). By combining both of these information sources, a better estimate of the target location can be obtained.

Figure: USRP software-defined radios used for the data acquisition

Objective
This Master’s thesis will provide a proof-of-concept of a joint AOA/TDOA estimation system. The student will have to design an experiment that allows joint estimation of AOA and TDOA using software-defined radios, and conduct the experiment. Various types of anchor deployments will have to be investigated to test various configurations. The experiment results will then have to be processed, by first analyzing AOA and TDOA separately, and then seeing how these two can be combined to improve localization accuracy.

Supervisors: Prof. François Quitin, Cédric Hannotier

Information : François Quitin (fquitin@ulb.be), Cédric Hannotier (Cedric.Hannotier@ulb.ac.be)

Students : ELEC, INFO
Design of a road user tracking system for smart cities

Motivation
Smart cities entail the real-time monitoring of traffic in urban environments. A promising approach for estimating the positions and speeds of targets (pedestrians, bikes, and cars) is the combination of different technologies, such as the detection of WiFi transmitters and radar system. The challenge is to combine all the different information sources in a reliable way, while also taking into account prior knowledge such as information about the roads, sidewalks and bikepaths.

Figure: example of a tracking filter that enables to correct for imperfect GPS data

Objective
This Master’s thesis will investigate how a system using RF transmitter localization and radar can track a road user. The information fusion of both systems will be done using well-established tracking algorithms (such as Kalman filters or particle filters). The student will also need to integrate information about the road layout in the tracking filter to provide better estimate of the road user location. The proposed algorithm will be tested in a simulation environment, and if successful, will be evaluated on experimental data.

Supervisors: Prof. François Quitin, Jean-François Determe

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Students: EM, ELEC, INFO
Contribution à l’upgrade des capteurs de l’expérience CMS (LHC) : test et caractérisation des capteurs au silicium et de leur chaîne de mesure
(in collaboration with Inter University Institute for High Energies)

Motivation :
Deux mémoires sont proposés dans le cadre de l’upgrade de l’expérience CMS (Compact Muon Solenoid) auprès du collisionneur proton-proton du CERN, le LHC. Pour cet upgrade, environ 2000 senseurs au silicium connectés à de l’électronique intégrée lue par fibre optique seront assemblés à Bruxelles à l’Institut Interuniversitaire des Hautes Energies (ULB-VUB). La production commencera en 2022 et est précédée d’une phase intense de prototypage.

Objectifs
Le premier MFE consistera à réaliser des tests détaillés des performances des premiers prototypes assemblés à Bruxelles, à des fins de validation et de caractérisation. Ces tests pourront être réalisés à l’aide des sources de particules chargées suivantes : muons cosmiques, électrons d’une source radioactive, faisceaux de particules. L’efficacité de détection, le rapport signal / bruit, l’uniformité de la réponse pourront être mesurés.
Les senseurs peuvent aussi fournir de l’information en temps réel, et la conformité de cette information avec l’information fournie en temps différé sera vérifiée.
Enfin, les senseurs peuvent mesurer l’impulsion des particules. Les différentes sources d’imprécision de cette mesure seront étudiées expérimentalement ainsi que par des simulations.

Un second sujet est de contribuer au développement des dispositifs de test permettant les études des prototypes, et en particulier le développement et la caractérisation de la chaîne électronique de lecture des senseurs. Ces dispositifs sont typiquement basés sur des cartes
équipées de puissants FPGA, compatibles avec le standard industriel x-TCA, qui communiquent avec l’électronique intégrée des senseurs via des liens optiques dits « radhard » conçus par le CERN. Ces dispositifs sont continuellement mis à jour avec l’arrivée des versions finales des différents composants électroniques. Pour tester les prototypes de senseurs, il faudra aussi vérifier l’intégrité de la chaîne d’électronique (par exemple l’intégrité de la communication optique) et implémenter toutes les fonctionnalités nécessaires pour tester les senseurs et mesurer leurs performances.

**Promoteurs :** Frédéric Robert, Pascal Vanlaer/Gilles De Lentdecker

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**Etudiants :** ELEC, PHYS
Implementation of wireless temperature monitoring system for JUNO backend card
(in collaboration with Inter University Institute for High Energies)

Motivation
At the Interuniversity Institute for High Energies (IIHE), we have been developing and assembling particle detectors for decades, especially for the CMS experiment of the Large Hadron Collider (LHC, CERN).
Now we are building a 20000 channel readout system for a neutrino detector (JUNO) under construction in China, it requires around 150 backend cards to collect trigger data from 7000 front-end units at a speed of 125Mbps. A temperature monitoring system is critical for stable long term operation. A board equipped with esp32 mcu has been designed and assembled, which needs to be programmed.

Objective
The main objective is the implementation of temperature monitoring on a custom designed board based on esp32 microcontroller.

The candidate will:
- Implement I2C interface in free-rtos environment
- Obtain temperature data from sensors on backend card
- Communicate with center server through wifi-mesh
- Implement power switch in case of failure happen to one of the redundant power supplies
- Implement XVC interface in free-rtos in order to remote update firmware for FPGA

Student's profile
- Student in engineering school, preferably in electronic related fields.
- Experienced in digital board design, MCU or FPGA programming.
- Good knowledge of C, Arduino, esp32, freertos, python
- Mastery of English (main language used in MFE)
- Autonomy
- Creativity, deductive skills, integration in a project team

Promotors: Frédéric Robert, Yifan Yang, Barbara Clerbaux

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Yifan Yang yang.yifan@ulb.ac.be (detailed content)

Students: ELEC, PHYS